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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS TX 75265

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HAWRANEK,S	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 11

Application Number: 09/092,115
Filing Date: June 05, 1998
Appellant(s): HANRATTY ET AL.

Carlton H. Hoel, Reg. No. 29,934
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 10/23/00.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-4 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,139,904	*Auda et al.*	*Aug. 18, 1992*
5,798,555	*Mishra et al.*	*Aug. 25, 1998*
5,525,542	*Mania et al.*	*Jun. 11, 1996*

S. Wolf, "Silicon Processing for the VLSI ERA Volume 2- Process Integration" (1986), pp. 278-286

(10) Grounds of Rejection

Claims 1-4 are rejected under 35 U.S.C. 103(a). This rejection is set forth in prior Office Action, Paper No. 7, clarified and duplicated for convenience as follows:

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Auda et al. (US Pat No. 5,139,904) and Wolf et al..

Auda et al. in figs. 1-5 and related discloses a method of fabrication of an integrated circuit whereby patterning a first layer of a resist on a layer of gate material (fig. 2a, 17a) to define gate locations these gates can be used in FETs (col.1, lines 15-20); reducing the line width of said patterned layer of resist (fig. 2c); using said reduced line width patterned resist as an etch

mask to form gates from said layer of a gate material (fig. 2d). The purpose for using reduced line width patterned resist for gates is to, "control the polysilicon line widths smaller than conventional UV photolithography equipment can achieve on standard photoresist layers. (col. 1, 15-20).

Auda et al. does not explicitly disclose forming a layer of dielectric on the gates patterning a second layer of photoresist to define interconnects without a reduction in line width to form interconnects over gates. (e.g., forming interconnects to connect the device to the "outside" world using conventional process steps.)

However, these conventional process are notoriously obvious as shown by Wolf et al. (pp. 280). Wherein the interconnects (e.g., CVD Tungsten (fig. 4-58)(contact the device to the "outside" world) are formed by forming a layer of dielectric (e.g., PECVD SiO_2 layer, pg. 280, line 2) on the gates. Next, forming a blanket layer of CVD Tungsten (W) on the dielectric layer, followed by patterning a second layer of photoresist (not shown in fig. 4-58, however, is inherent characteristic of the CVD TUNSTEN(W) interconnect formation used to fill the via) on the CVD W layer and then etching the CVD W layer with the patterned photoresist layer in order to form the CVD W interconnect into the desired pattern as shown in figure 4-58.

Because there is no need for a reduced sized interconnect, conventional photoresist and etching techniques would be have been employed. (e.g., without the use of a reduced photoresist and hence the no reduced linewidth in the interconnect) In addition, figure 4-58 clearly shows a gate with a smaller linewidth than the CVD W interconnect, further evidence of no reduced photoresist application.

Wolf shows that these interconnects are conventional way to make contact the "outside" world. It would have been obvious to one of ordinary skill in the art at the time of the invention

to use the conventional process of forming interconnects as shown by Wolf with Auda for its disclosed intended purpose of forming interconnects in order to obtain connection to the "outside" world.

Furthermore, the use of reduced photoresist and non reduced photoresist has been shown to be obvious as applied above. Therefore, the choice of using a mixed strategy would merely be optimization of the result effective variable (e.g., reducing the photoresist and linewidth) and is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious).

2. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mishra et al.(U.S. Pat. No. 5,798,555) in view of Auda et al (U.S. Pat. No. 5,139,904) and Maniar et al.(U.S. Pat. No. 5,525,542).

Mishra et al. teaches in figs. 1-17 and related text a method of forming an integrated circuit gate by pattering a first layer of resist (fig. 2a, 48) on a dummy gate material to define gate locations forming a dummy gate structure with photo resists (fig. 2e, 48), reducing the width of dummy gate (fig. 2e-2f); forming a dielectric layer over gate (fig. 2g, 66,64); removing dummy gate; a metal contact is deposited into region (fig. 2g, 68). Thereby, forming a T-Shaped gate electrode with a photo resists. It is held, absent evidence to the contrary, that T-shaped gate electrode is formed with a photoresist without a reduction as is conventional in the art. The T-

shaped gate electrode provides a better contact with more surface area, thereby, providing an improved contact as demonstrated by Mishra et al.

Mishra et al. lacks anticipation for using a reduced photoresist and utilizing antireflective layers.

Auda et al., discloses supra, and using a reduced photoresists in order to obtain smaller geometries and better control of the gate line widths. (col. 1, 15-20).

It would have been obvious to one of ordinary skill in the art to have modified Mishra et al. with the teachings of Auda et al. in order to obtain a smaller gate geometries and have better control as taught by Auda et al.

Examiner takes official notice that the use of anti-reflective coatings over a reflective conductive layers is notoriously obvious and is convention in the art as shown by Maniar et al. In which Maniar et al. discloses the use of antireflective coatings to avoid reflected radiation back to portions of the photoresist which cause inconsistencies in patterns of the imaged photoresist.

Therefore, it would have been obvious to one of to have modified Auda et al. and Mishra et al. with Maniar et al. in order to obtain a more accurate profile with the use of antireflective coating as taught by Maniar et al.

The use of reduced photoresist and non reduced photoresist has been shown to be obvious as applied above. Therefore, the choice of using a mixed strategy would merely be optimization of the result effective variable (e.g., reducing the photoresist) and is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges

within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious).

(11) Response to Argument

Arguments regarding the double patent rejection of claim 1 are persuasive and rejection of paper 7 has been overcome.

Regarding claims 1-3 Appellants assert the references fail to suggest such a use of both reduced and nonreduced linewidths. However, such a mixed a strategy is made obvious by the combination of Auda et al. with Wolf. Wolf shows in figures 4-58 line widths of the gate electrode and the CVD tungsten interconnect are different. Clearly the use of a reduced photoresist would not have been necessary in the formation of the CVD tungsten interconnect evidence by the relative size of the interconnect to the gate electrode. Auda et al. discloses the use of a reduced photoresist in order to obtain better geometries of polysilicon gate electrodes (e.g., reduced line-widths) (col. 1, lines 15-20), however, does not suggest to employ these methods in the formation of interconnects.

Appellants agree that the use of interconnect lithography, dummy gate electordes, antireflective coating, and photoresist reduction are well known in the art. (pg. 3 of appeal brief) However, argue one would only exclusively apply the reduced photoresist application or the conventional non-reduced photoresist application in making a device. This is contrary to Auda et al. teachings, wherein the use of a reduced photoresist is a solution to forming miniaturized short channel polysilicon gate FETs in which smaller geometries are desired. Auda does not appear to suggest the use of this technique in the formation of conventional interconnects.

Appellants assert there is no suggestion of the mixed use of photoresist (e.g., conventional and reduced). However, there is a suggestion to used the reduced photoresist for the formation of gate electrodes. See Auda et al. (col. 1, lines 15-20). Auda et al. is relied upon for said teachings. It would be implausible to use the reduced photoresist for the conventional interconnects without any explicit motivation. Therefore, one of ordinary skill in the art would have been motivated to use the teachings of Auda et al. for there disclosed intended purpose, to form the gate electrode only. The conventional techniques (e.g., with the reduced photoresist) in the formation of the interconnects would have been applied without any teachings in order to form contacts to the "outside" world as shown by Wolf.

Appellant asserts the double patenting rejection essentially repeats the rejections based on the references. Analogous reasoning as applied above is applicable to the double patenting rejection. Wherein the use of reduced photoresist and the non-reduced photoresist is an obvious variation and design choice. One of ordinary skill in the art would apply the reduced photoresist to gate electrodes in order to obtain smaller geometries, however, when these geometries are not necessary in the formation of interconnects such an application would be unwarranted.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Scott J. Hawranek
January 16, 2001

LONG PHAM
PRIMARY EXAMINER